A Simple Mathematical Model for Clocked QCA Cells

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***Abstract*—In this paper Equivalent circuit of a three input majority gate for clocked implementation state is presented. The output voltage of a clocked logical QCA (quantum-dot cellular automata) circuit which is a three-input majority gate is simulated. For this scope a model simulated with MATLAB is used to simulate clocked QCA circuits. By using this model, it is possible to design and simulate clocked combinational QCA and hybrid circuits including QCA and other nano devices. Combined theoretical and experimental studies, show that the QCA-based circuits potentially lead to circuits with densities that are 3-4 orders of magnitude beyond what CMOS (Complementary metal–oxide–semiconductor) circuits can provide. It should dissipate very little power, and could be clocked at an extremely high frequency (adiabatically at 1 THz). Clocking in QCA provides power gain, reduces power dissipation, and provides a means for memory features in the cells and QCA latches. By introducing clocked control of the QCA cell, computational pipelining can be achieved**.

***Keywords*—clocked QCA circuit model, majority voting gate, tunnel junction.**

I. INTRODUCTION

Day by day along with decreasing of the CMOS technology scaling below the 100nm, some defects such as ultrathin gate leakage and doping fluctuations arise and result in increasing of power density level. These defects finally would end the down scaling trend of CMOS technology. In the recent years novel technologies like SET (single electron device), RTD (resonant tunneling devices), nano-tube, nano-wire and QCA (quantum-dot cellular automata) are greatly researched to find a nano replacement for previous VLSI (Very-large-scale integration) technology.

QCA is based upon the encoding of binary information in the charge configuration within quantum dot cells. A fundamental QCA is made up of four quantum dots which are located on vertices of a square; also there are two electrons in a QCA cell that can tunnel between dots inside the cell. The electrons must be located on the opposite corners of square according to the Coulomb repulsion in ground states. In this case the polarization of the cell is P=+1 or P=-1. It is shown in Fig.1. The ground states could be used to represent the logic '0' and '1'. QCA cells interact because the charge configuration of one cell alters the charge configuration of the next cell. Based on basic QCA cells, it has been demonstrated and designed QCA wires, QCA majority voter, inverter, and more complicated circuits such as full-adder, H-memory structure, and 12-bit microprocessor [1-3].

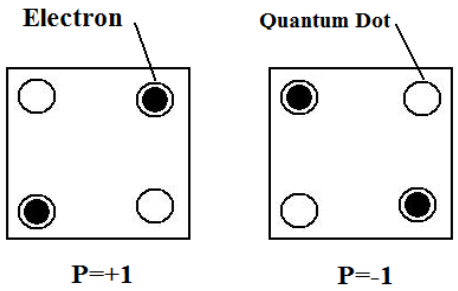

Figure 1. standard QCA cells showing the polarizations of two ground states.

Polarizations of the four–dot cell described above is controlled by the input signal applied to it, However, to make large scale circuit using QCA devices, it is desirable to be able to control switching using a clock signal. Combined theoretical and experimental studies, show that clocking in QCA provides power gain, and provides a means for memory features in the cells reduces power dissipation [4], and QCA latches. Metal quantum dot based implementations of clocked computational schemes were proposed in [5-7] and various experiments have highlighted the key features of clocked QCA architectures [5–10]. Clocking is done by electro statically switching the cell from a null state, in which cell holds no binary information, through a switching state, in which the cell state is influenced by its neighbors, to a locked state, in which the state is independent of its neighbors.

In a three-input majority gate, clocking would increase the stability to the operation of a majority logic performance.

By applying a clock signal to QCA circuits, the states of QCA change with clock operation. As shown in Fig. 2, with applying clock, electron locates at one of the dots with respect of input voltage sign. Even when inputs are grounded, the state remains fixed and includes one of the following states: 0.-1, 1 or 1,-1, 0. When the clock signal is off, and input voltages are grounded, the state becomes 0,0,0 that means null state. The null state is used to control the switching between the other states, and can only be maintained with the external influence of clock signal. Therefore by using of this property, we can attain to QCA latches that would lock at one state by applying zero clock.

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The proposed article is organized as follows: the clocked QCA behavior is introduced in the next section based on metal-dot based physical implementation. Imn the third section the clocked QCA mathematical model is presented, and in section IV the three input majority voting gate simulation for the clocked implementation using MATLAB is illustrated.

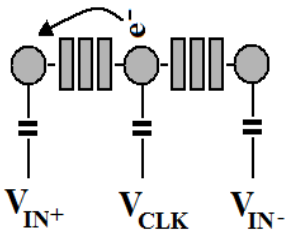

Figure 2. When the clock signal is on, electron tunnels to the dot with positive potential

II. CLOCKED QCA

By applying clock signal, a middle dot is added on each side of the cell. When the clock signal is large and attractive, the electron is moved onto the middle dots, as shown in Fig. 3(b). That means null state of the cell; it contains no bit information. If the clock signal shifts to become large and repulsive, the charges move to the corners and the cell switches to a "0" or "1" state depending on the states of neighboring cells (Fig. 3(a), 3(c)). A large repulsive clock signal locks the cell in its state, and acts as a barrier to charge tunneling [11-12].

Clocking controls the information flow at the circuit, and also provides true power gain in QCA devices. Signal energy is lost in environment due to unavoidable dissipative processes (e.g. phonon emission) as information moves from one stage to another stage the information will be lost. Thus each stage must have actual power gain, augmenting a weak input signal to restore logic levels. In clocked QCA the clock signal provides energy without flow of the current. The clock leads to restore cells to the fully polarized "1" and "0" states [12-13].

III. THE CLOCKED QCA MATHEMATICAL MODEL

Many simulations and experiments have been arranged to demonstrate behavior of the QCA cells. Our model consists of mathematical equations which are used in clocked QCA circuits. In our simulation the 'push-pull' signal is used to polarize the input dots that the sign of the voltage on one input dot is opposite to the one on another input dot, and by measuring the output voltages, the polarization direction of the output dots is determined. A circuit model of a basic QCA cell is shown in Fig. 4(a).

We consider a three-input majority gate that a clock signal is applied to it (see Fig. 4(b)).

First we consider the left half of circuit and calculate the voltages of the quantum dots in this zone, and by using them as the inputs of right half try to attain the out put. T_1 is a tunneling junction and the two black dots represent two quantum dots.

The required electrostatic energy to move an electron from island m to island n is given by [10]:

$$\Delta E = -e(v_n - v_m) + \frac{(C_{mm}^{-1} - 2C_{mn}^{-1} + C_{nn}^{-1})e^2}{2}, \qquad (1)$$

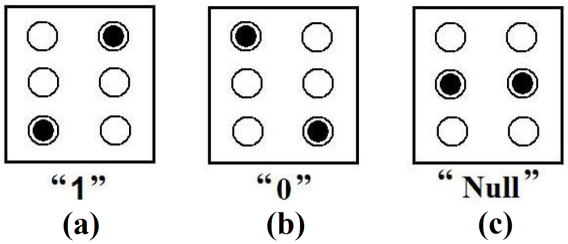

Figure 3. A clocked QCA cell that is a six-dot cell.(b) varying the potential of the middle dots or pulling the electrons onto the middle dots leads to a "null" state of the cell, (a) ,(c) and by varying the potential of the middle dots or by pushing the electrons off of the middle dots state of the cell become"1" or "0".

Where, C_{mm} and C_{nn} are capacitances of nodes m and n with respect to the ground, and C_{mn} is the capacitance between them. V_m and V_n are the voltages on island m and n before the tunneling of the electron from node m to node n. Considering a simple case, there is only one extra electron in one pair of quantum dots. Therefore, the probability that the node m holds one electron while the node n has no electron and probability that the node m holds no electron while node n has one electron are related as [14]:

$$P_{m=1,n=0}\Gamma_{m\to n} = P_{m=0,n=1}\Gamma_{n\to m}, \qquad (2)$$

Here, $\Gamma_{m\to n}$ is the tunnel rate for an electron tunnelling from island m to island n.

Based on the orthodox theory the tunnel rate is formulated as [10]:

$$\Gamma(\Delta E) = \frac{\Delta E}{e^2 R_T\left(\exp(\Delta E / K_B T) - 1\right)}, \qquad (3)$$

Where, R_T is the tunnel resistance, k_B is Boltzmann's constant, T is temperature, and E is the delta energy calculated from (1). C_{mk} (m from 1 to 3) is the corresponding input capacitance for each input with voltage source V_{mk} of island m. It is assumad that the total capacitance of island m is equal to the Island n. By using the simple electrostatics, the following equations are obtained:

$$V_{m=1} = \frac{(\sum V_{mk}C_{mk} - e)C_S + (\sum V_{nk}C_{nk})C_{T_1}}{C_s^2 - C_{T_1}^2} \qquad (4)$$

$$V_{n=0} = \frac{(\sum V_{mk}C_{mk} - e)C_{T_1} + (\sum V_{nk}C_{nk})C_S}{C_s^2 - C_{T_1}^2}, \qquad (5)$$

$$V_{m=0} = \frac{(\sum V_{mk}C_{mk})C_S + (\sum V_{nk}C_{nk} - e)C_{T_1}}{C_s^2 - C_{T_1}^2} \qquad (6)$$

$$V_{n=1} = \frac{(\sum V_{mk}C_{mk})C_{T_1} + (\sum V_{nk}C_{nk} - e)C_S}{C_s^2 - C_{T_1}^2}, \qquad (7)$$

Where V_m=1 is the voltage of node m with the extra electron and V_m=0 is the voltage of node i with no extra electron. C_S is the total capacitance of node m and m. C_{TI} is the capacitance of tunneling junction T_1, The tunnel junctions act as capacitors that couple the potential on one dot to that of others and provide a path for quantum-mechanical tunneling and the average voltages of island m and n are given by:

$$V_m = P_{m=1,n=0}V_{m=1} + P_{m=0,n=1}V_{m=0}, \quad (8)$$

$$V_n = P_{m=0,n=1}V_{n=1} + P_{m=1,n=0}V_{n=0}, \quad (9)$$

This model has the capability of desirable clock controlling for designing the complicated asynchrony circuits. Using this ability, we can simulate the clock controlled circuits. Also we can use the proposed model in hybrid QCA and other nano-device circuits.

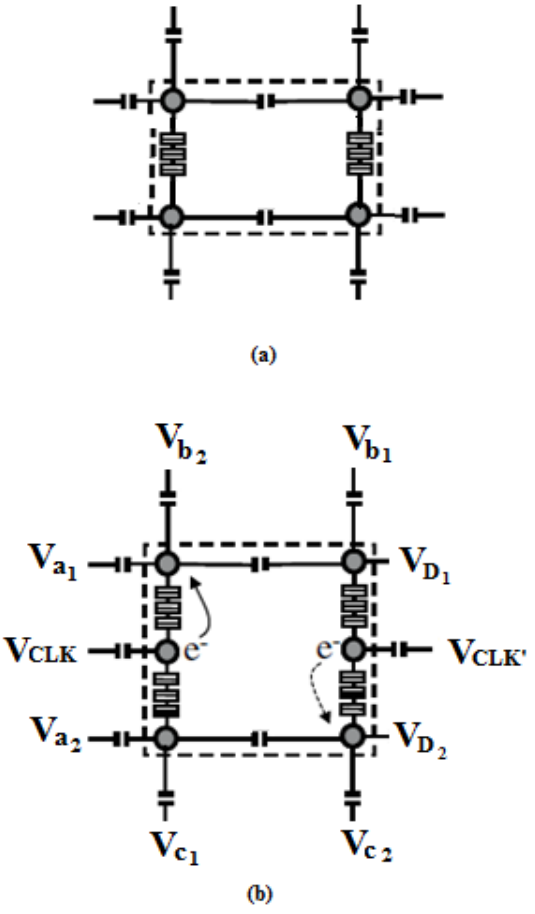

Figure 4.(a) A Realization of a basic QCA cell composed of quantum dots, tunnel junctions and capacitances. (b) Shematic diagram of a clocked three-input majority gate circuit.

IV. SIMULATIONS RESULTS

By using of this simple model, we simulated a three-input clocked majority gate, which is one of the basic QCA gates, it is shown in Fig. 5. In the other word, this is an static circuit model which we used to simulate the QCA clocked circuits by using the equivalent circuit shown in Fig. 4.

Cells A, B, C are the input cells and D is the output cell that is influenced by polarization state of input cells with the logic function of:

$$F(A,B,C) = AB + BC + AC, \quad (10)$$

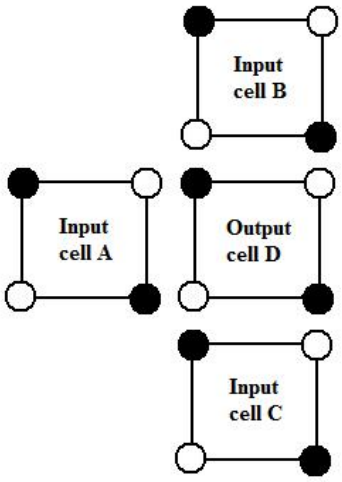

Figure 5. the input cells and output cells of a majority voting gate.

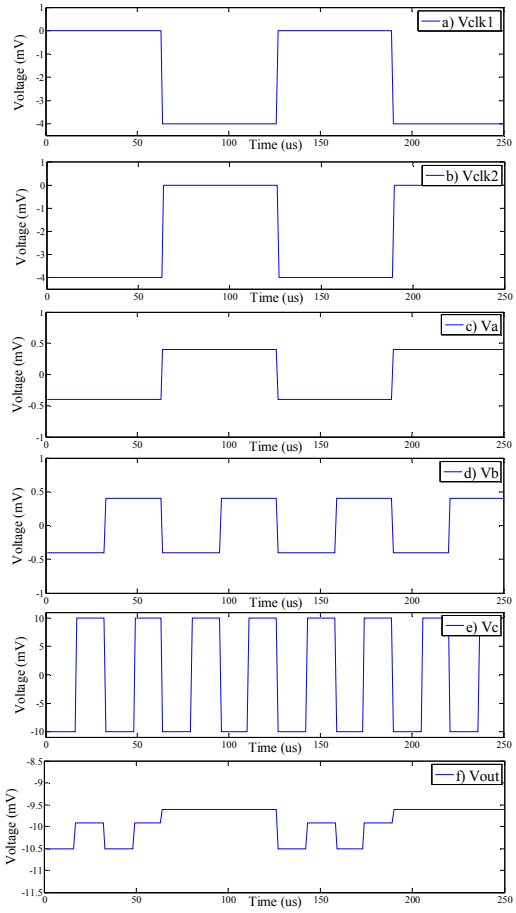

Figure 6. Simulation results of a clocked QCA majority gate. (a) clock voltage of left half of circuit. (b) clock voltage of right half of circuit. (c) output voltage of input cell A. (d) output voltage of input cell B. (e) output voltage of input cell C. (f) output voltage of output cell D.

By applying a clock signal to these circuits, the state of output cell changes with clock operation. When clock signal is on, electron locates at one of the dots with respect of input voltage sign. Even when inputs are grounded, the state remains fixed and locked to previous state.

The values of capacitors and resistors used in this simulation are obtained from Ref. [15].

First consider the clocked circuit model shown in Fig. 4(b), two clock signals with different phase applied to the circuit, one for right half of the circuit and one for left half of it.

As can be seen from simulation results (Fig. 6); when clock signal of right half of circuit is "off" the output voltages are fixed, and when this clock signal is "on" output voltages changes with varying inputs. The output transition of the majority gate according to the input transitions when the clock signal is high can be formulated according to the (10). The duration of On and Off is long enough to observe the impact of the clock at the output.

V. CONCLUSION

In this paper we focused on clocked QCA circuits and mentioned their operation and presented a simple circuit model for analyzing them. The circuit model of a clocked majority gate is shown and simulation results by applying the model are obtained and shown in previous sections. This model has the capability of desirable clock controlling for designing the complicated asynchronous circuits. Using this ability, we can simulate the clock controlled circuits. A clocked QCA circuit model is presented, and the simulation results using the mathematical model are correctly extracted. It is addressed that by using the circuit model and the presented mathematical model the QCA based circuits could be simulated by MATLAB simulator.

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